08/04/04

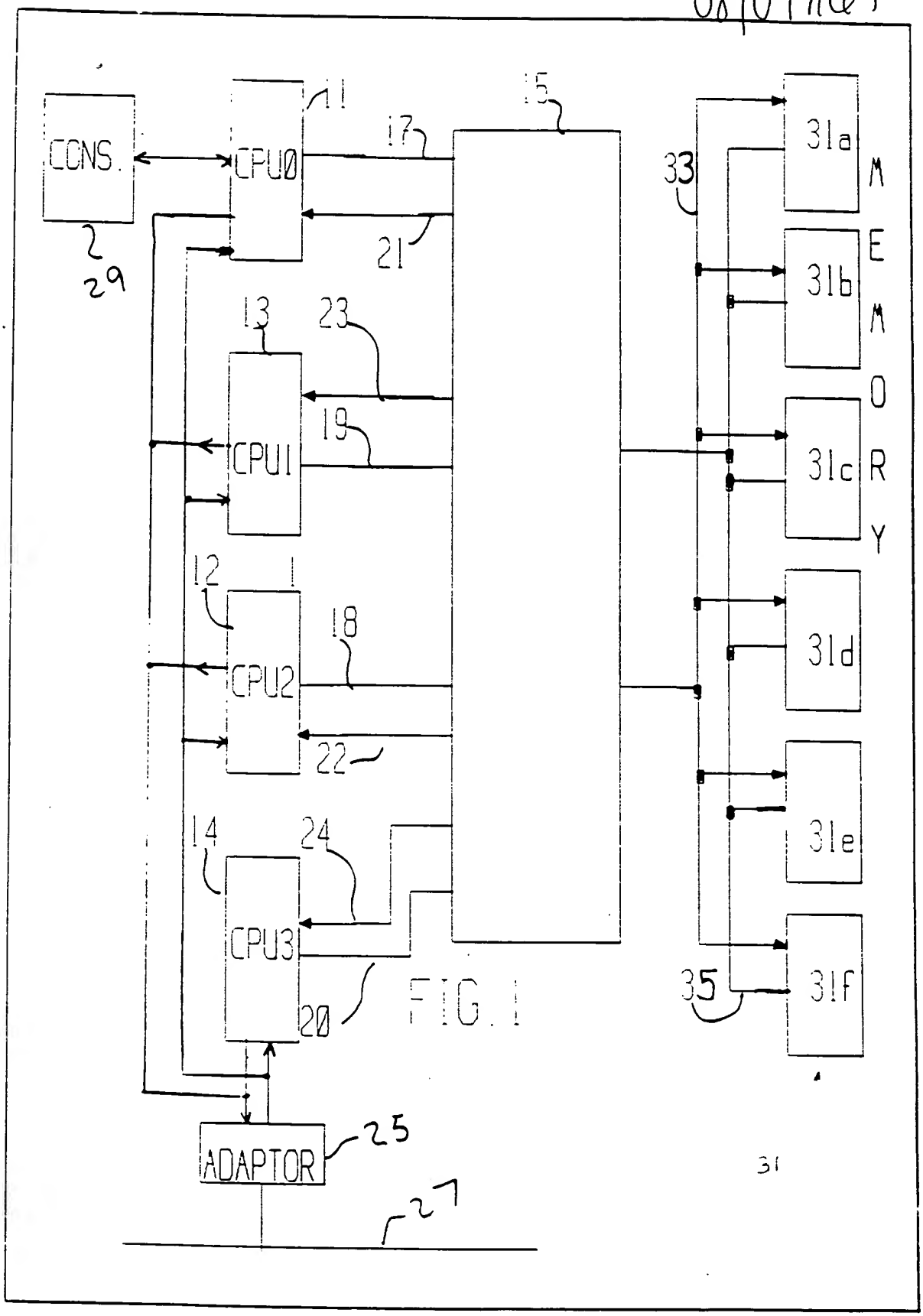
CONS.
CPU0
CPU1
CPU2
CPU3
ADAPTOR
11
15
17
21
29
13
23
19
12
1
18
22
14
24
20
25
27
31a
31b
31c
31d
31e
31f
33
35
MEMORY
31

FIG. 1

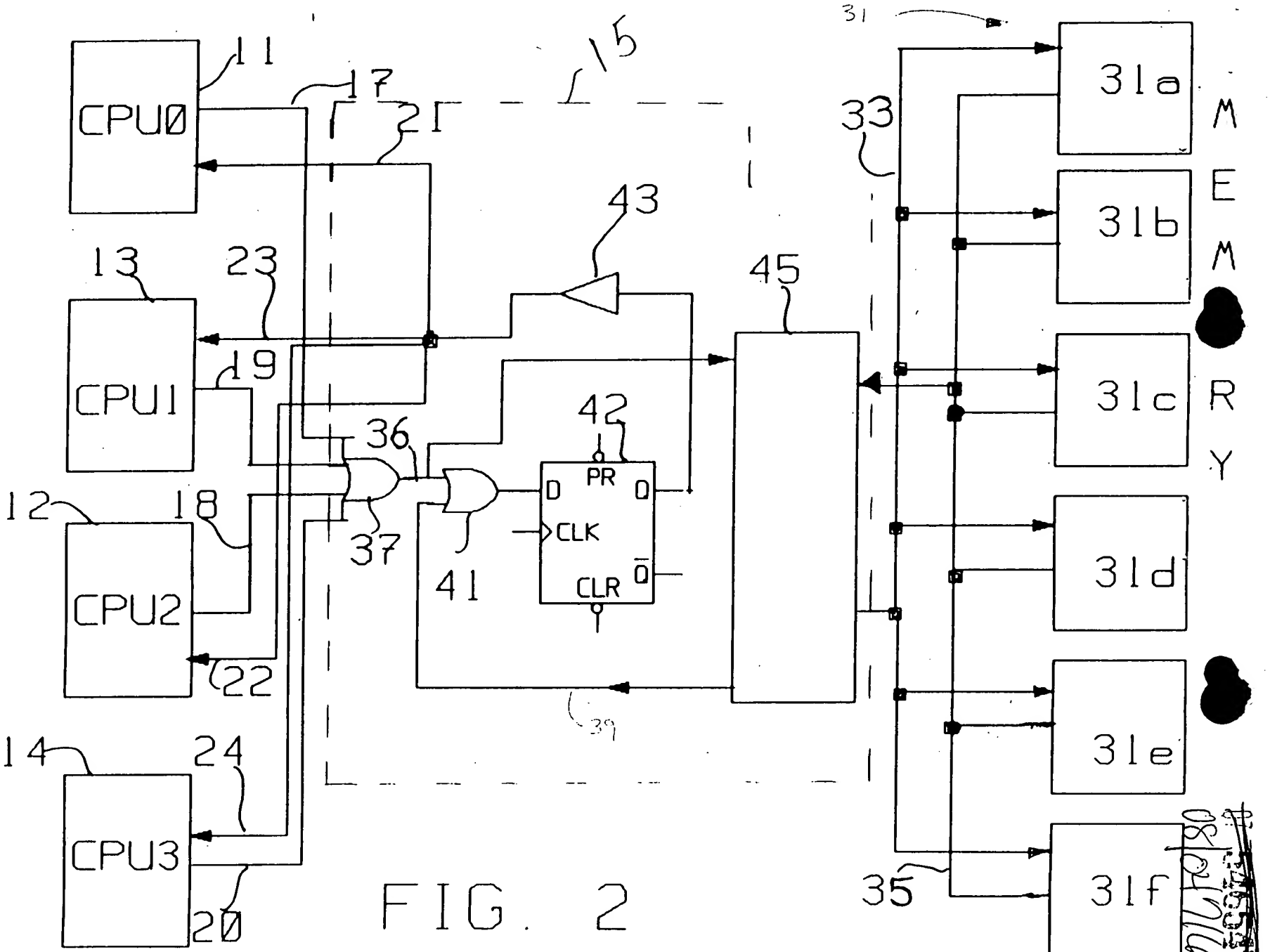
CPU0
CPU1
CPU2
CPU3
11
13
12
14
17
19
18
20
21
22
23
24
15
31
31a
31b
31c
31d
31e
31f
33
35
MEMORY
43
45
42
36
37
41
PR
CLK
CLR
D
Q
$\bar{Q}$
39

FIG. 2

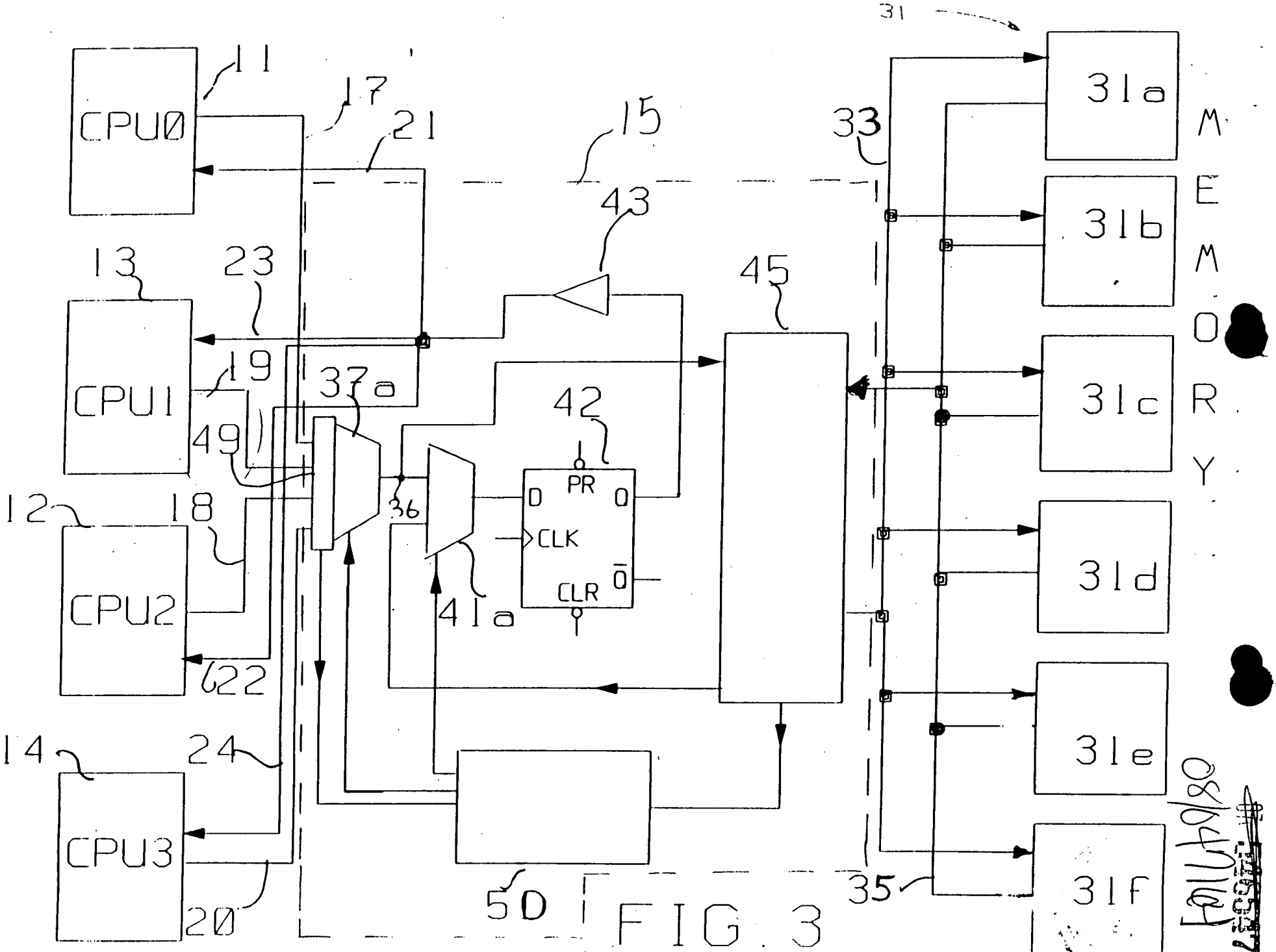
CPU0
CPU1
CPU2
CPU3
11
17
21
15
31
33
31a
31b
31c
31d
31e
31f
MEMORY
13
23
43
45
19
37a
42
49
PR
D
Q
CLK
CLR
12
18
36
41a
22
14
24
20
50
35

FIG. 3

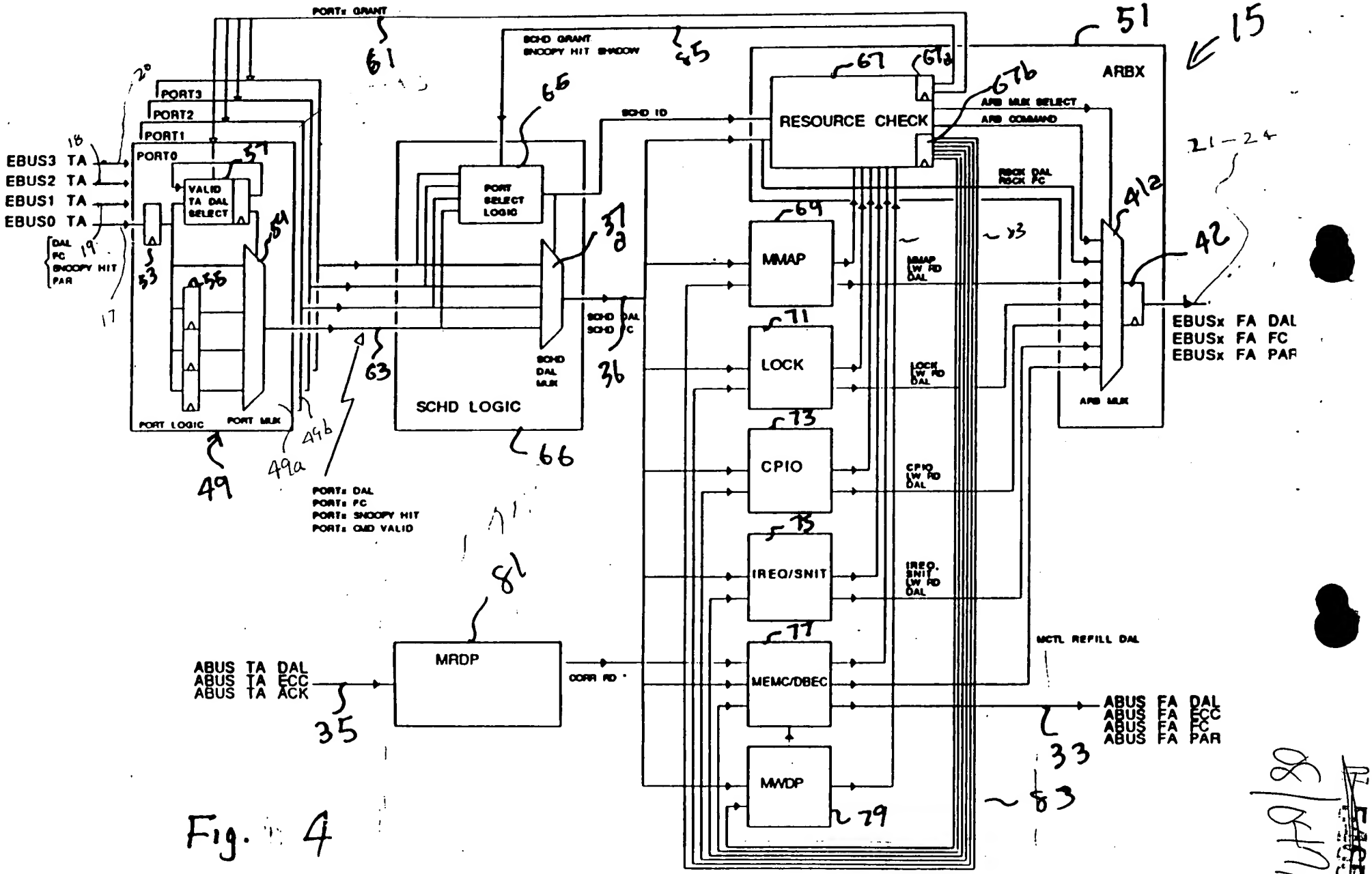
PORT= GRANT
61
SCHD GRANT
SNOOPY HIT SHADOW
65
51
15
ARBX
67
67a
67b
RESOURCE CHECK
ARB MUX SELECT
ARB COMMAND
SCHD ID
66
PORT3
PORT2
PORT1
PORT0
EBUS3 TA
EBUS2 TA
EBUS1 TA
EBUS0 TA
DAL
FC
SNOOPY HIT
PAR
VALID
TA DAL
SELECT
PORT
SELECT
LOGIC
SCHD
DAL
MUX
SCHD DAL
SCHD FC
PORT LOGIC
PORT MUX
SCHD LOGIC
49
49a
49b
63
66
PORT= DAL
PORT= FC
PORT= SNOOPY HIT
PORT= CMD VALID
MMAP
LOCK
CPIO
IREQ/SNIT
MEMC/DBEC
MWDP
MMAP LW RD DAL
LOCK LW RD DAL
CPIO LW RD DAL
IREQ. SNIT LW RD DAL
MCTL REFILL DAL
ARB MUX
EBUSx FA DAL
EBUSx FA FC
EBUSx FA PAR
ABUS FA DAL
ABUS FA ECC
ABUS FA FC
ABUS FA PAR
MRDP
CORR RD
ABUS TA DAL
ABUS TA ECC
ABUS TA ACK
35
33
83
79
69
71
73
75
77
81
42
42a
53
56
57
18
19
20
17
21-24

Fig. 4

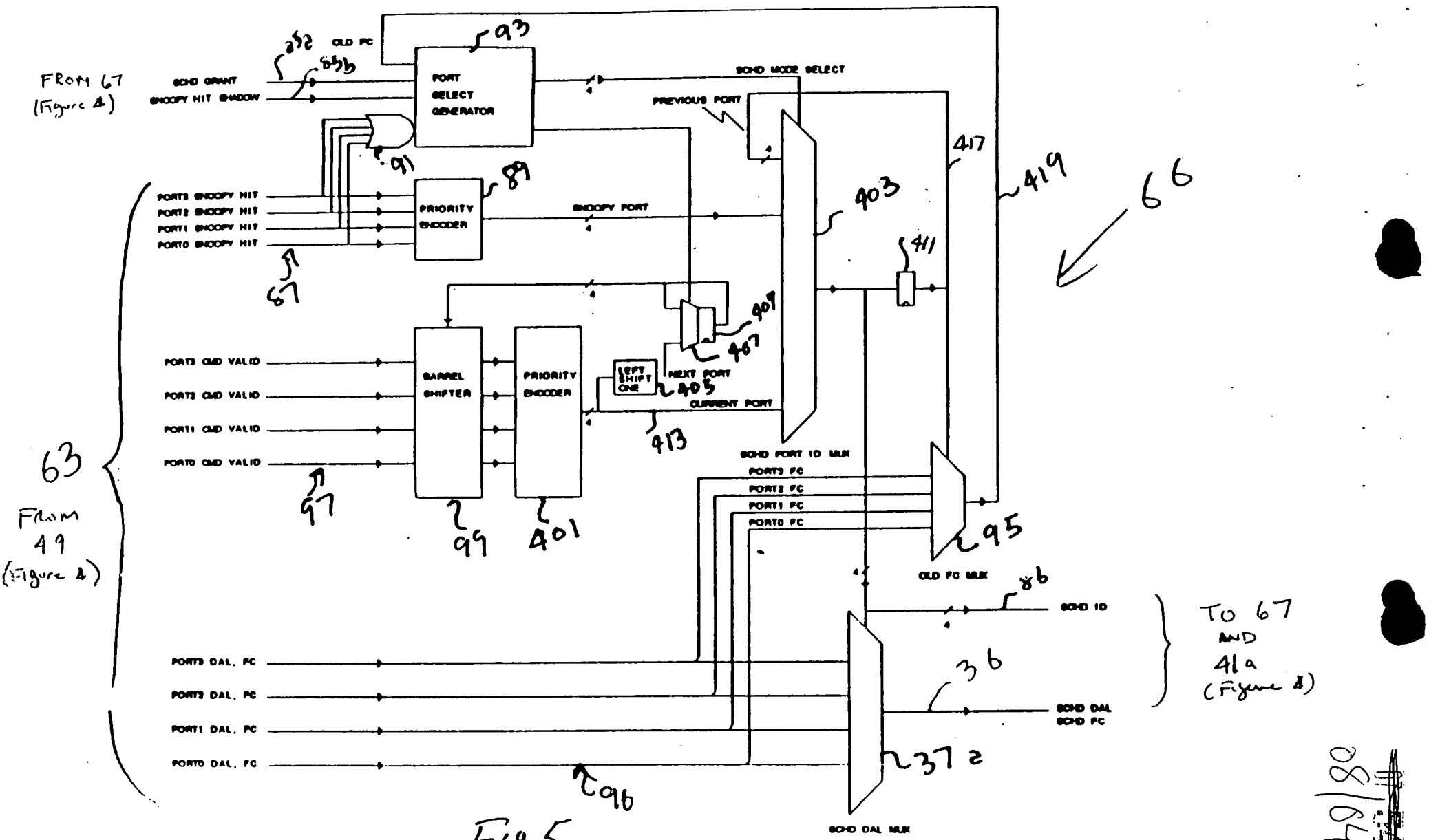
FROM 67 (Figure 4)
OLD FC
SCHD GRANT
SNOOPY HIT SHADOW
PORT SELECT GENERATOR
SCHD MODE SELECT
PREVIOUS PORT
PORT3 SNOOPY HIT
PORT2 SNOOPY HIT
PORT1 SNOOPY HIT
PORT0 SNOOPY HIT
PRIORITY ENCODER
SNOOPY PORT
PORT3 OLD VALID
PORT2 OLD VALID
PORT1 OLD VALID
PORT0 OLD VALID
BARREL SHIFTER
PRIORITY ENCODER
LEFT SHIFT ONE
NEXT PORT
CURRENT PORT
SCHD PORT ID MUX
PORT3 FC
PORT2 FC
PORT1 FC
PORT0 FC
OLD FC MUX
SCHD ID
PORT3 DAL, FC
PORT2 DAL, FC
PORT1 DAL, FC
PORT0 DAL, FC
SCHD DAL
SCHD FC
SCHD DAL MUX
63
From 49 (Figure 4)
TO 67 AND 41a (Figure 4)
66
67
91
89
403
417
419
411
409
407
405
413
97
99
401
95
86
36
37a
96

Fig. 5

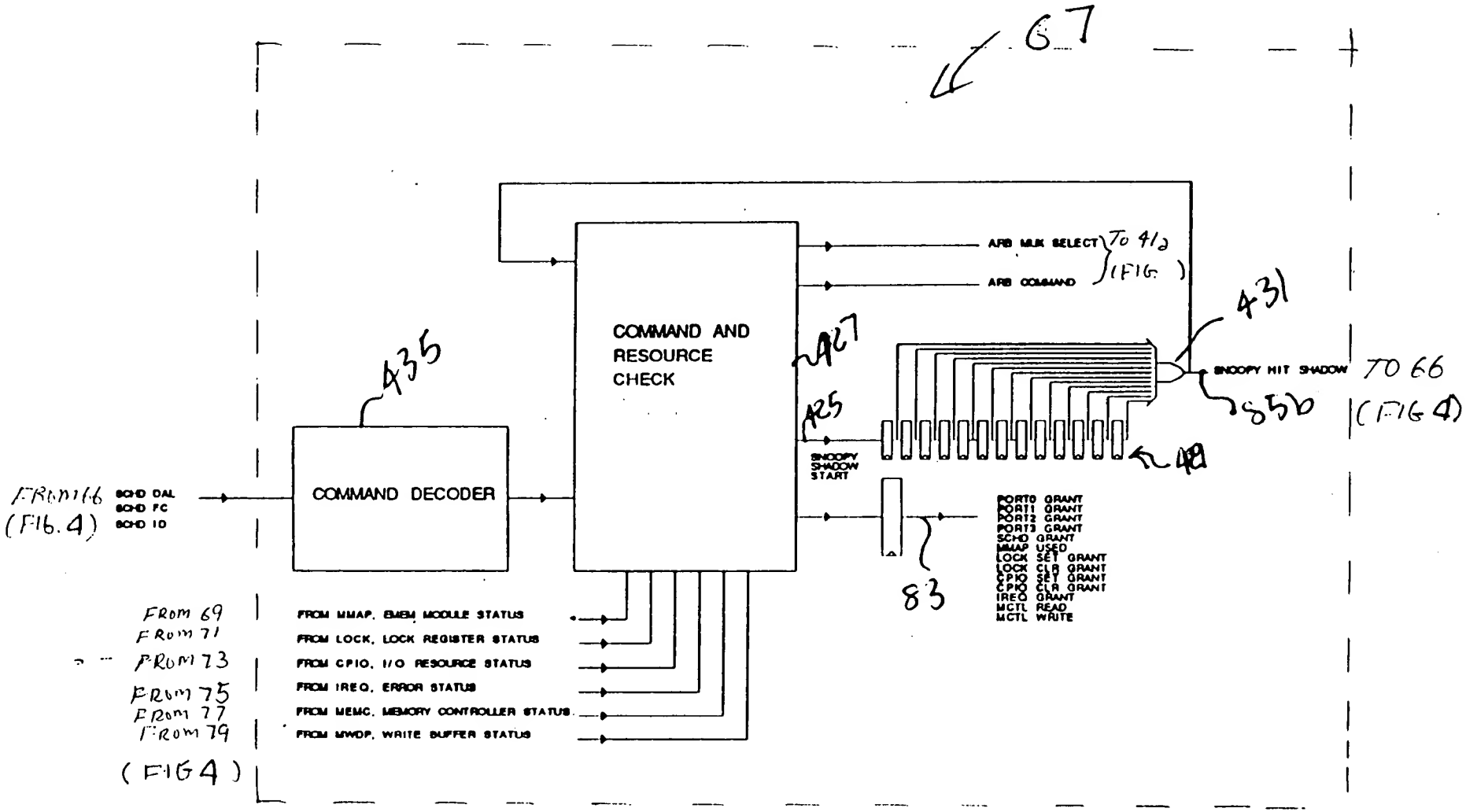
67
COMMAND AND RESOURCE CHECK
COMMAND DECODER
435
427
425
431
ARB MUX SELECT
ARB COMMAND
To 412 (FIG.)
SNOOPY HIT SHADOW
TO 66 (FIG 4)
850
SNOOPY SHADOW START
83
PORT0 GRANT
PORT1 GRANT
PORT2 GRANT
PORT3 GRANT
SCHD GRANT
MMAP USED
LOCK SET GRANT
LOCK CLR GRANT
CPIO SET GRANT
CPIO CLR GRANT
IREQ GRANT
MCTL READ
MCTL WRITE
FROM 66 (FIG. 4)
SCHD DAL
SCHD FC
SCHD ID
FROM 69
FROM 71
FROM 73
FROM 75
FROM 77
FROM 79
(FIG 4)
FROM MMAP, EMEM MODULE STATUS
FROM LOCK, LOCK REGISTER STATUS
FROM CPIO, I/O RESOURCE STATUS
FROM IREQ, ERROR STATUS
FROM MEMC, MEMORY CONTROLLER STATUS
FROM MWDP, WRITE BUFFER STATUS

Fig. 6

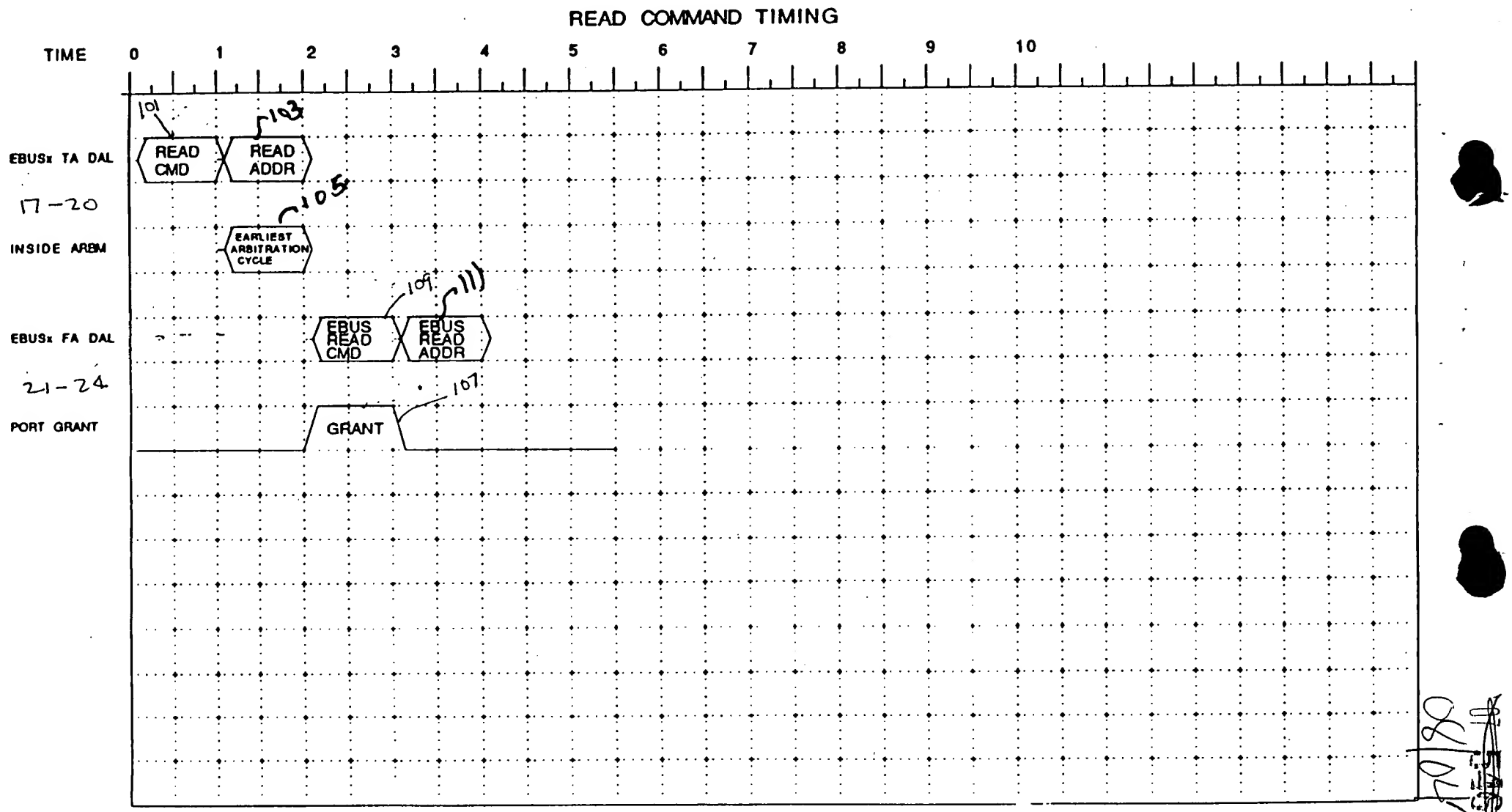
READ COMMAND TIMING
TIME
0
1
2
3
4
5
6
7
8
9
10
EBUSx TA DAL
17-20
INSIDE ARBM
EBUSx FA DAL
21-24
PORT GRANT
101
103
105
107
109
111
READ CMD
READ ADDR
EARLIEST ARBITRATION CYCLE
EBUS READ CMD
EBUS READ ADDR
GRANT

Fig 7

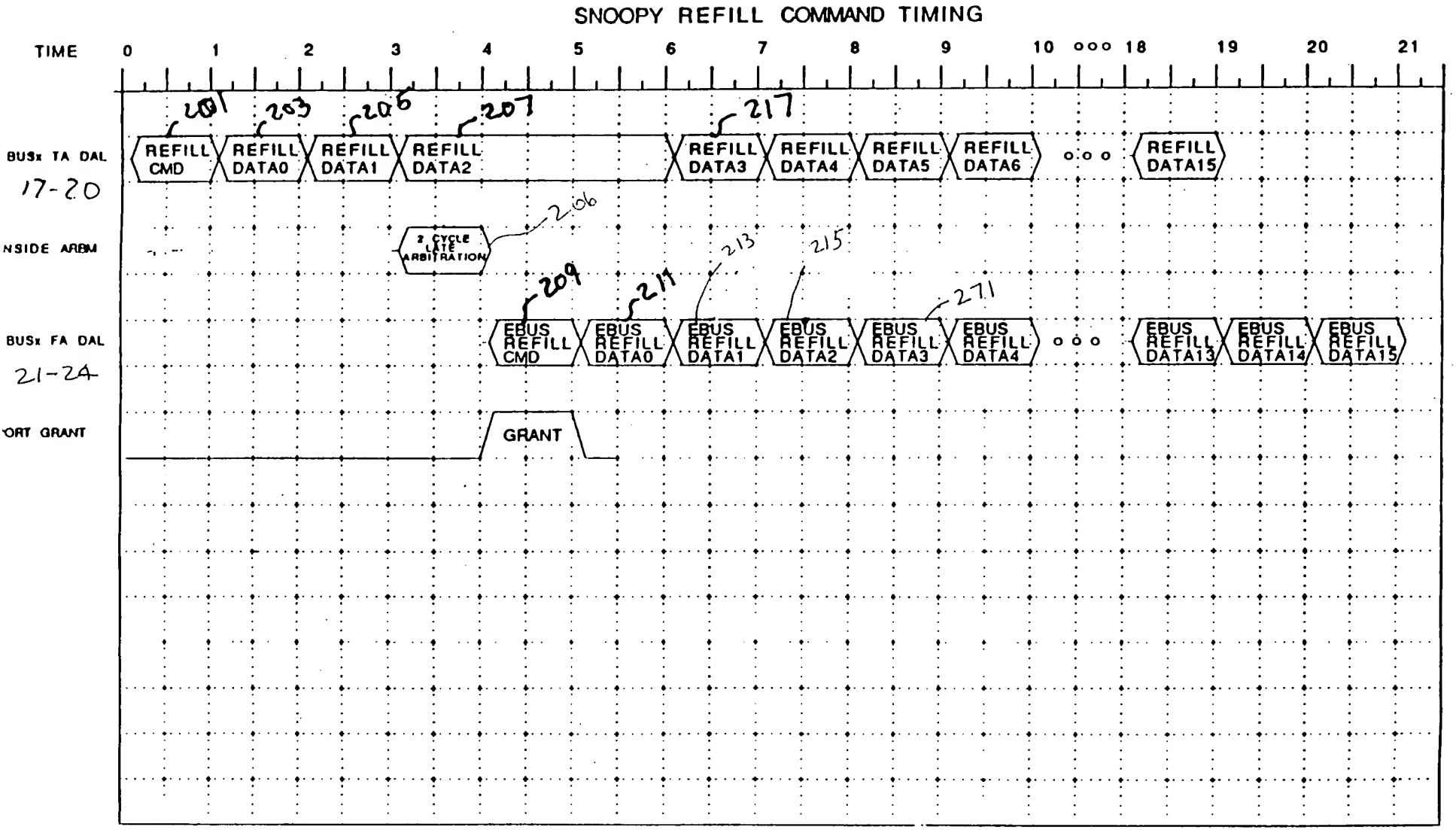
SNOOPY REFILL COMMAND TIMING
TIME
0
1
2
3
4
5
6
7
8
9
10
18
19
20
21
201
203
205
207
217
BUSx TA DAL
17-20
REFILL CMD
REFILL DATA0
REFILL DATA1
REFILL DATA2
REFILL DATA3
REFILL DATA4
REFILL DATA5
REFILL DATA6
REFILL DATA15
NSIDE AREM
2 CYCLE LATE ARBITRATION
206
209
211
213
215
271
BUSx FA DAL
21-24
EBUS REFILL CMD
EBUS REFILL DATA0
EBUS REFILL DATA1
EBUS REFILL DATA2
EBUS REFILL DATA3
EBUS REFILL DATA4
EBUS REFILL DATA13
EBUS REFILL DATA14
EBUS REFILL DATA15
ORT GRANT
GRANT

Fig 8

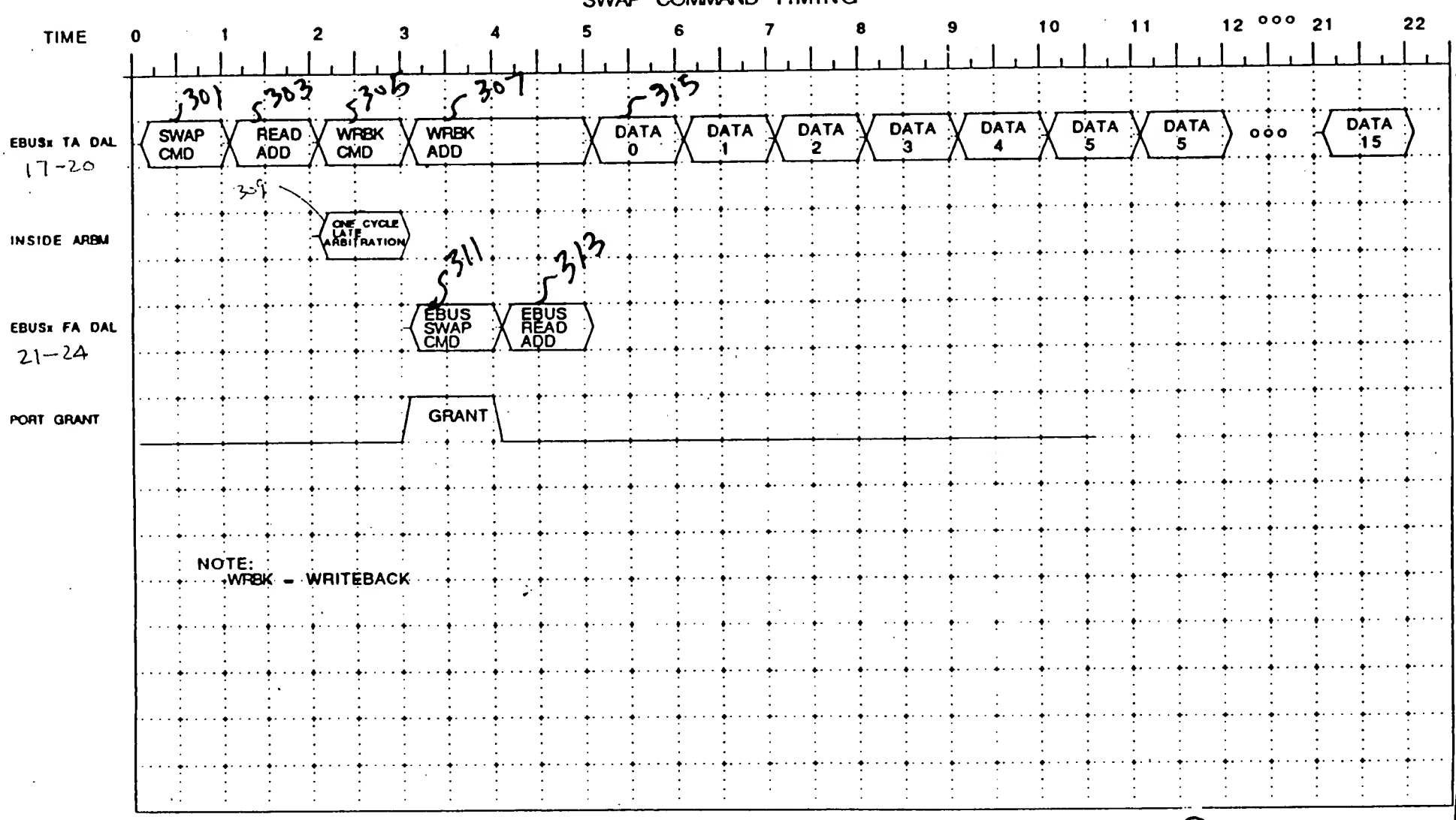
SWAP COMMAND TIMING
TIME
0
1
2
3
4
5
6
7
8
9
10
11
12
ooo
21
22
EBUSx TA DAL
17-20
SWAP CMD
READ ADD
WRBK CMD
WRBK ADD
DATA 0
DATA 1
DATA 2
DATA 3
DATA 4
DATA 5
DATA 5
ooo
DATA 15
301
303
305
307
315
INSIDE ARBM
309
ONE CYCLE LATE ARBITRATION
EBUSx FA DAL
21-24
311
313
EBUS SWAP CMD
EBUS READ ADD
PORT GRANT
GRANT
NOTE:
WRBK - WRITEBACK

Fig 9